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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,183	12/10/2003	Debendra Mallik	42P16843	8055

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

3/L

Office Action Summary	Application No.	Applicant(s)	
	10/733,183	MALLIK ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *10-19,43-52 and 2734* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,20-26 and 35-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species 2 in the reply filed on 01/09/2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 8, 35-39 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Radu et al. (US 6,956,285).

4. Regarding claims 1, Radu (e.g. fig. 1) shows an microelectronic device package, comprising: an electrically conductive lid 206 having an attachment surface; a substrate 202 having an attachment surface; at least one electrically conductive first interconnect 218 extending between the lid attachment surface and the substrate attachment surface; at least one microelectronic die 204 disposed between the lid attachment surface and the substrate attachment surface; and the substrate having at least one first conductive trace 222 extending between the electrically conductive first interconnect and the microelectronic die (col. 14/lls. 14-53).

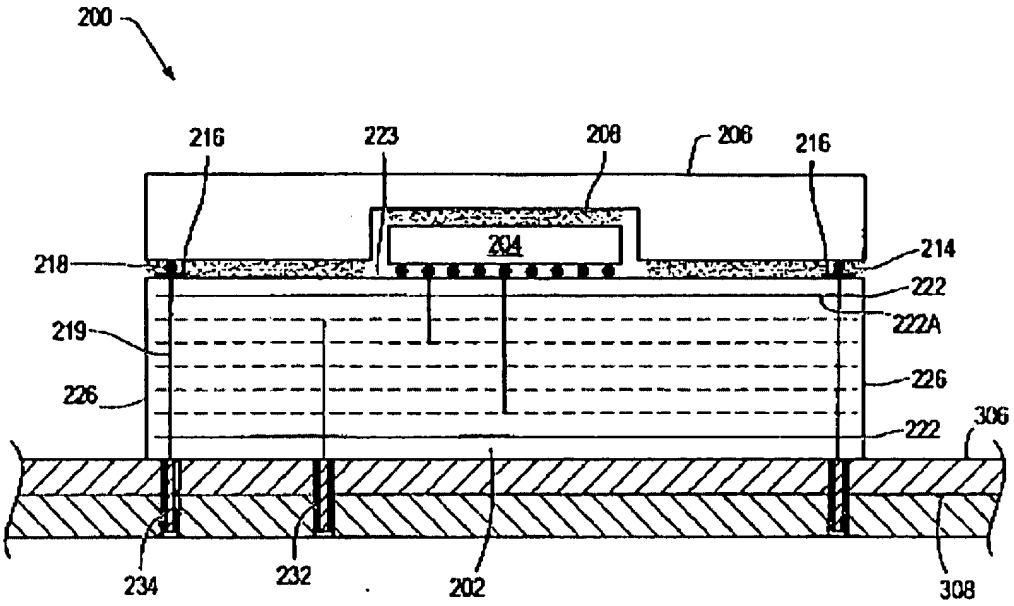


FIG. 2A

5. Regarding claim 2, Radu shows that the package includes first signal line in electrical communication with the electrical conductive lid (col. 3/lls. 1-5).

6. Regarding claim 3, Radu snows that the lid comprises a thermally conductive heat dissipation device 400 (e.g. fig. 5).

7. Regarding claim 4, Radu shows a thermal interface material 208 disposed between the heat dissipation device and the back surface of microelectronic die.

8. Regarding claim 5, Radu shows a socket (i.e. connecting holes of substrate 306/308 having a first surface (e.g. top surface), a second surface (e.g. bottom surface) opposing to the first surface; an a recess extending into the socket first surface. Also, the substrate and the microelectronic die substantially residing in the socket recess; and a portion of the lid 355 extending proximate to the socket first surface (e.g. fig. 5).

9. Regarding claim 6, Radu shows a first signal line 219 extending from the socket second surface to the socket first surface, wherein the first signal trace is in electrical contact with the lid.

10. Regarding claim 8, Radu shows a second signal line 232 extending from the socket second surface to the socket first surface, wherein the second signal trace is in electrical contact with the substrate.

11. Regarding claim 35, Radu (e.g. fig. 2A) shows a method of delivering at least one signal to a microelectronic die, comprising: providing an electrically conductive lid 206 having an attachment surface; providing a substrate 202 having an attachment surface; disposing at least one electrically conductive first interconnect 218 extending between the lid attachment surface and the substrate attachment surface; disposing at least one microelectronic die 204 between the lid attachment surface and the substrate attachment surface; providing at least one first conductive trace 222 extending between the electrically conductive first interconnect and the microelectronic die; and delivering a signal to the electrically conductive lid (col. 14/lls. 14-53).

12. Regarding claim 36, Radu snows that the lid comprises a thermally conductive heat dissipation device 400 (e.g. fig. 5).

13. Regarding claim 37, Radu shows a thermal interface material 208 disposed between the heat dissipation device and the back surface of microelectronic die.

14. Regarding claim 38, Radu shows a socket (i.e. connecting holes of substrate 306/308 having a first surface (e.g. top surface), a second surface (e.g. bottom surface) opposing to the first surface; an a recess extending into the socket first surface. Also,

the substrate and the microelectronic die substantially residing in the socket recess; and a portion of the lid 355 extending proximate to the socket first surface (e.g. fig. 5).

15. Regarding claim 39, Radu shows a first signal line 219 extending from the socket second surface to the socket first surface, wherein the first signal trace is in electrical contact with the lid.

16. Regarding claim 41, Radu shows a second signal line 232 extending from the socket second surface to the socket first surface, wherein the second signal trace is in electrical contact with the substrate

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 7, 9, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radu et al. (US 6,956,285) in view of Fujino (JP- 2001319997).

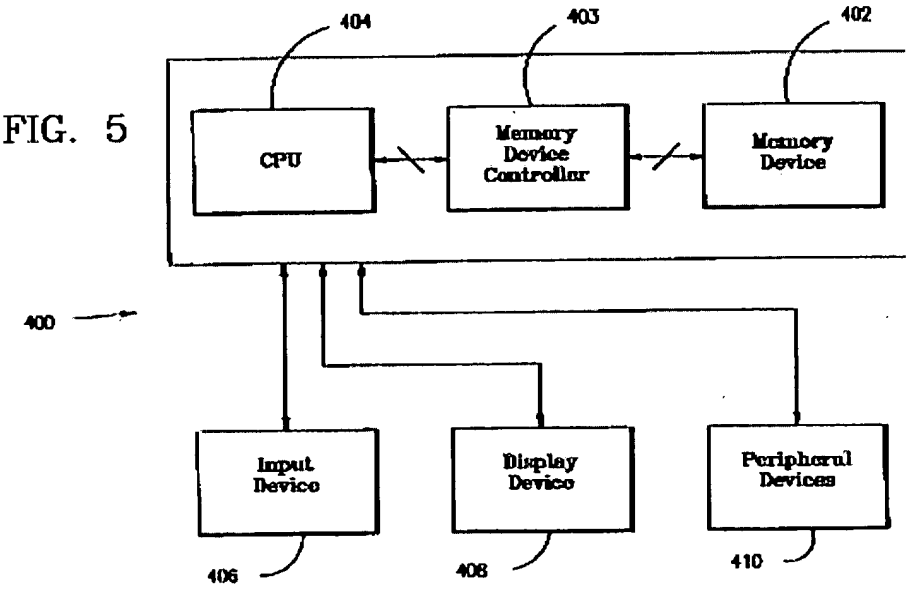
19. Regarding claims 7, 9, 40 and 42, Radu shows most aspects of the instant invention except at least one external contact contacting the at least one first/second signal line proximate tot the second socket surface. Nevertheless, Fujino (e.g. fig. 1) shows a substrate 2 having external contact contacting at least one first/second signal line 5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include, in the invention disclosed by Radu, at least one external contact contacting the at least one first/second signal line proximate to the second

socket surface as suggested by Fujino in order to provide an interconnection means that provide an excellent electrical performance while the connection inductance can be reduced.

20. Claims 20-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman (US 6,172,419) in view of Radu et al. (US 6,956,285).

21. Regarding claim 20, Kinsman shows most aspects of the instant invention including an electronic system 400, comprising: a microelectronic device package CPU 404 attached to and external substrate (e.g. fig. 4; 32), an input device 406 interfaced with the external substrate and a display device 406 interfaced with the external substrate.

FIG. 5



However, Kinsman does not show that the microelectronic package includes: an electrically conductive lid having an attachment surface; a substrate having an attachment surface; at least one electrically conductive first interconnect extending between the lid attachment surface and the substrate attachment surface; at least one

microelectronic die disposed between the lid attachment surface and the substrate attachment surface; and the substrate having at least one first conductive trace extending between the electrically conductive first interconnect and the microelectronic die. Nevertheless, Radu shows microelectronic device package (CPU) is attached to an external substrate 306 wherein the device package, comprising: an electrically conductive lid 206 having an attachment surface; a substrate 202 having an attachment surface; at least one electrically conductive first interconnect 218 extending between the lid attachment surface and the substrate attachment surface; at least one microelectronic die 204 disposed between the lid attachment surface and the substrate attachment surface; and the substrate having at least one first conductive trace 222 extending between the electrically conductive first interconnect and the microelectronic die (col. 1/lls. 26-28 & col. 14/lls. 14-53). According to Radu, this type of embodiment reduces or eliminates the electromagnetic interface that interferes with the individual performance of individual IC devices as well as the overall performance of the system (col. 1/lls. 12-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the microelectronic package (e.g. CPU) disclosed by Kinsman having an electrically conductive lid having an attachment surface; a substrate having an attachment surface; at least one electrically conductive first interconnect extending between the lid attachment surface and the substrate attachment surface; at least one microelectronic die disposed between the lid attachment surface and the substrate attachment surface; and the substrate having at least one first conductive trace extending between the electrically conductive first

interconnect and the microelectronic die as suggested by Radu to reduce/eliminate electromagnetic interface that interferes with the IC device individual performance as well as the overall performance of the system.

22. Regarding claim 21, Radu shows that the package includes first signal line in electrical communication with the electrical conductive lid (col. 3/lls. 1-5).

23. Regarding claim 22, Radu shows a socket (i.e. connecting holes of substrate 306/308 having a first surface (e.g. top surface), a second surface (e.g. bottom surface) opposing to the first surface; an a recess extending into the socket first surface. Also, the substrate and the microelectronic die substantially residing in the socket recess; and a portion of the lid 355 extending proximate to the socket first surface (e.g. fig. 5).

24. Regarding claim 23, Radu shows a first signal line 219 extending from the socket second surface to the socket first surface, wherein the first signal trace is in electrical contact with the lid.

25. Regarding claim 25, Radu shows a second signal line 232 extending from the socket second surface to the socket first surface, wherein the second signal trace is in electrical contact with the substrate.

26. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinsman (US 6,172,419) in view of Radu et al. (US 6,956,285) further in view of Fujino (JP- 2001319997).

27. Regarding claims 24 and 26, Kinsman in view of Radu shows most aspects of the instant invention except at least one external contact contacting the at least one first/second signal line proximate tot the second socket surface. Nevertheless, Fujino

(e.g. fig. 1) shows a substrate 2 having external contact contacting at least one first/second signal line 5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form in the system disclosed by Kinsman in view of Radu at least one external contact contacting the at least one first/second signal line proximate to the second socket surface as suggested by Fujino in order to provide an interconnection means that provide an excellent electrical performance while the connection inductance can be reduced.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Primary Examiner
Art Unit 2826